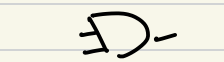
CS 315-01 Digital Logic Components

gates 

wires
inputs
outputs
splitter

combinational logic
outputs depend only on input
circuit is a DAG directed acyclic graph.

sum-of-products
boolean algebra equation → circuit

adder ripple-carry adder

circuits as components

Near term goal: static analysis

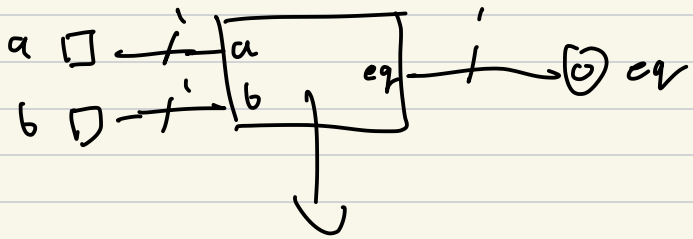
Comparator is $a == b$?

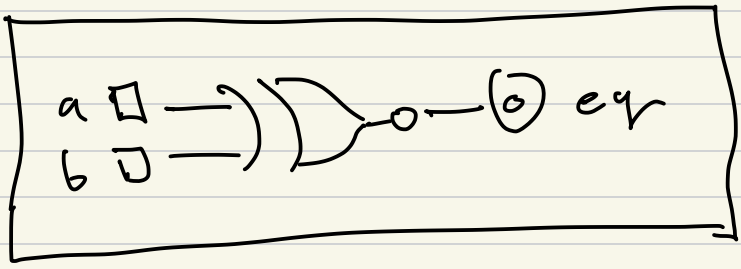
$$eq = (\bar{a} \cdot \bar{b}) + (a \cdot b)$$

a	b	eq?
0	0	1
0	1	0
1	0	0
1	1	1

XOR	$\overline{\text{XOR}}$	XNOR
0	1	1
1	0	0
1	0	0
0	1	1

1 bit comparator

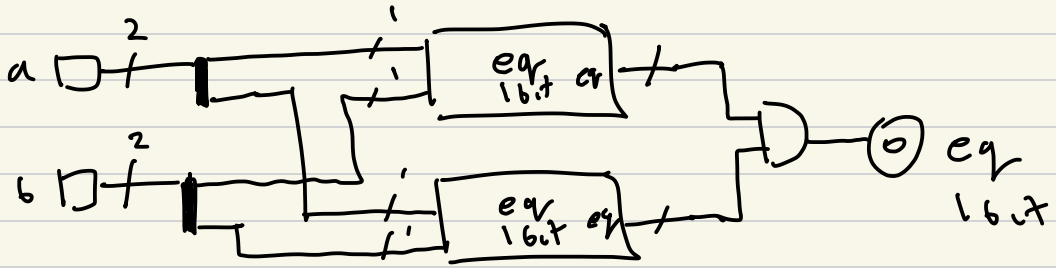




101 == 101

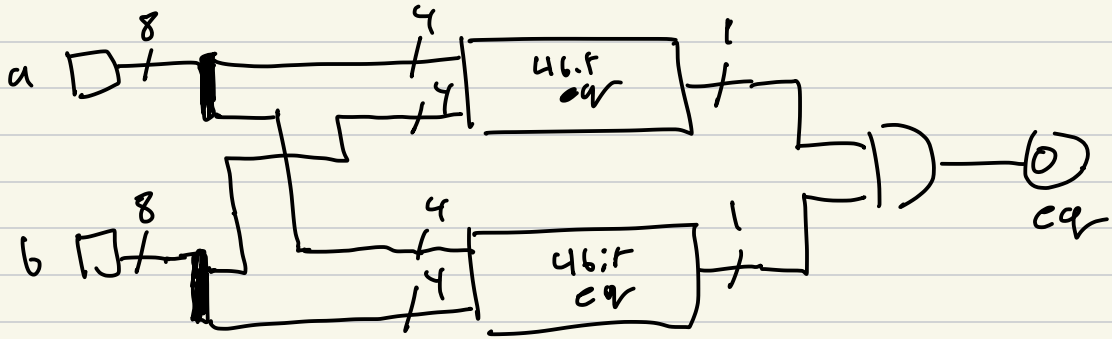
100 =/= 101

2-bit comparator

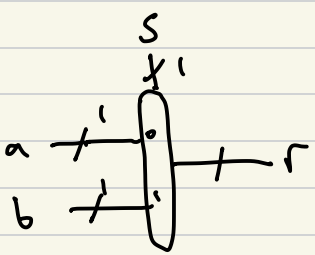


N-bit comparators

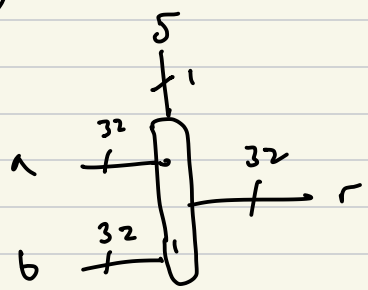
8 bit comparator



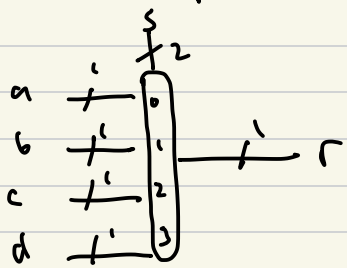
Multiplexor (MUX)



1 bit 2 input MUX



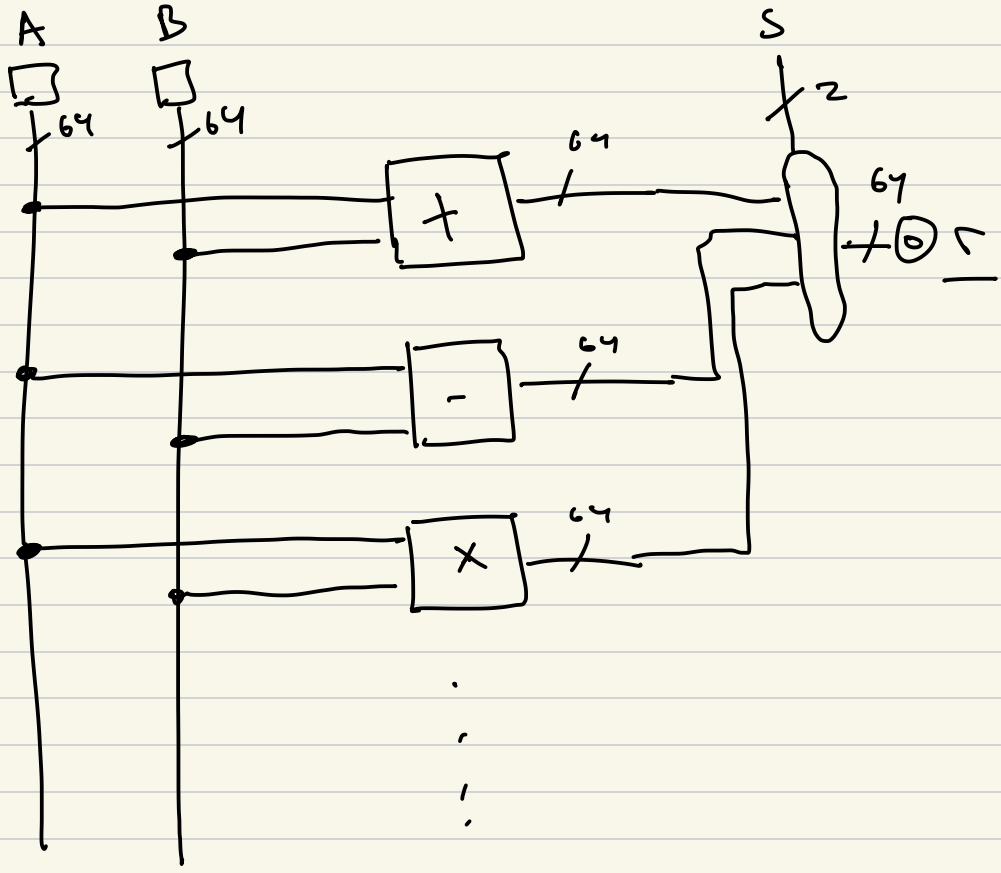
32 bit 2 input MUX



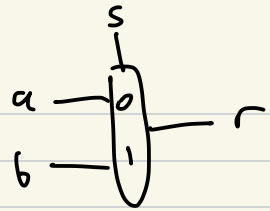
1 bit 4 input MUX

Uses of MUXes:

ALU Arithmetic Logic Unit



Implementing MUXes

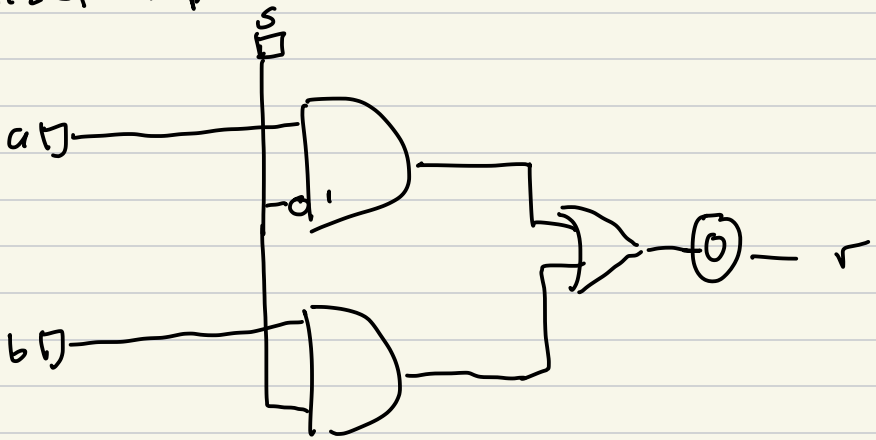


1 bit 2 input MUX

a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

$$r = (\bar{a} \cdot b \cdot s) + (a \cdot \bar{b} \cdot \bar{s}) + (a \cdot b \cdot \bar{s}) + (a \cdot b \cdot s)$$

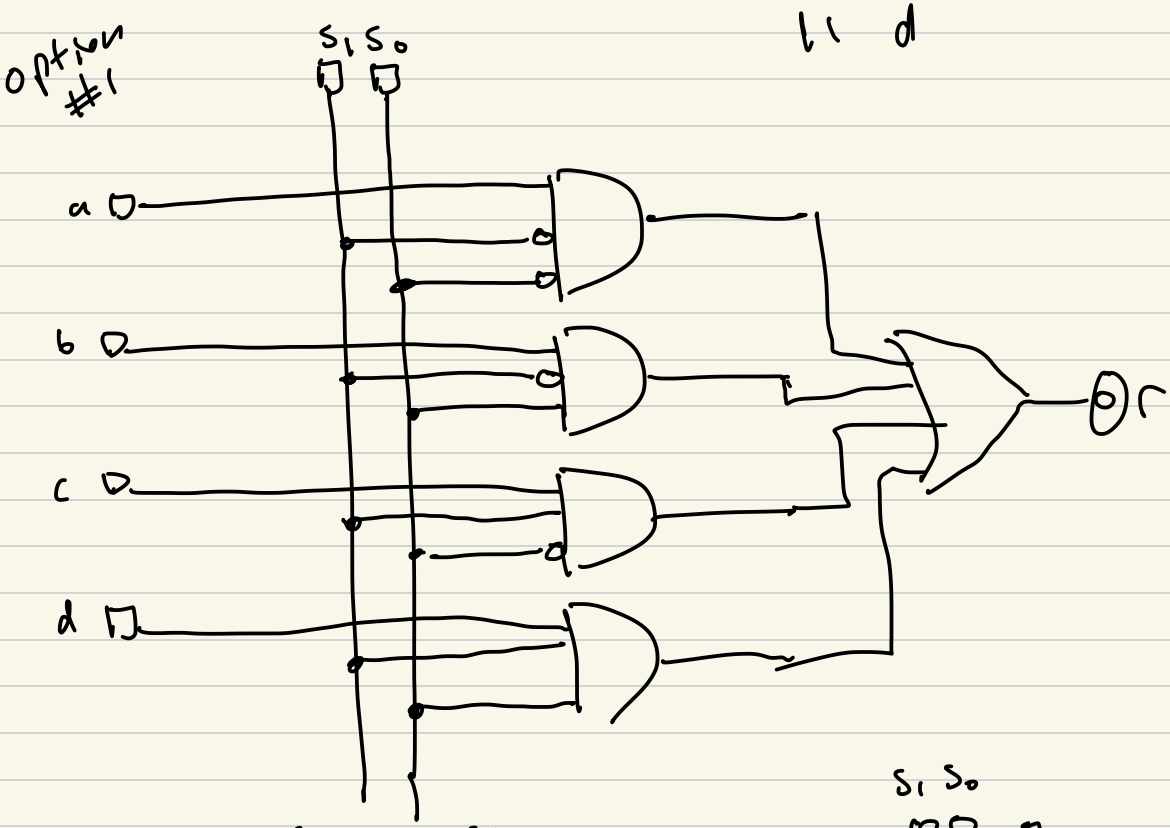
Direct implementation



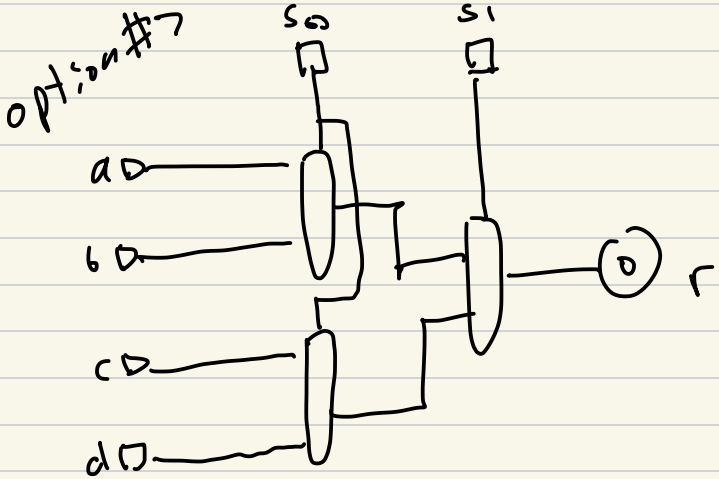
1 bit 4 input MUX

S_1	S_0	out
0	0	a
0	1	b
1	0	c
1	1	d

option #1

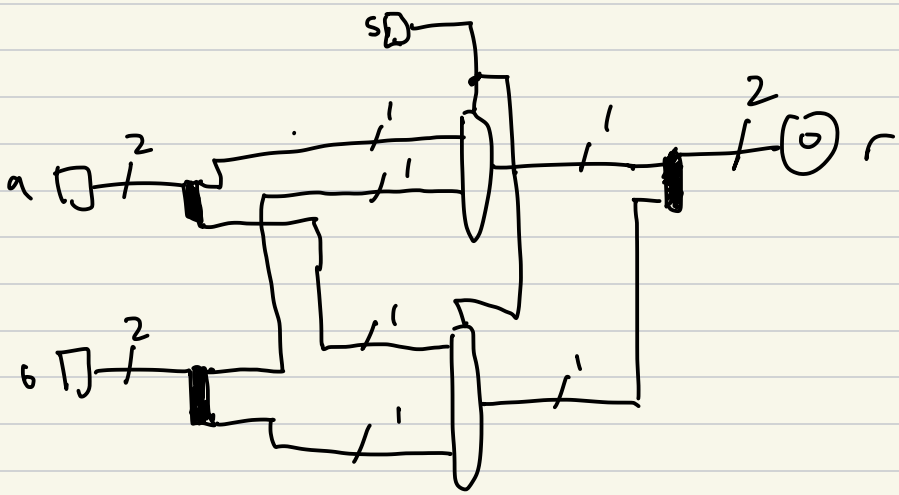


option #7

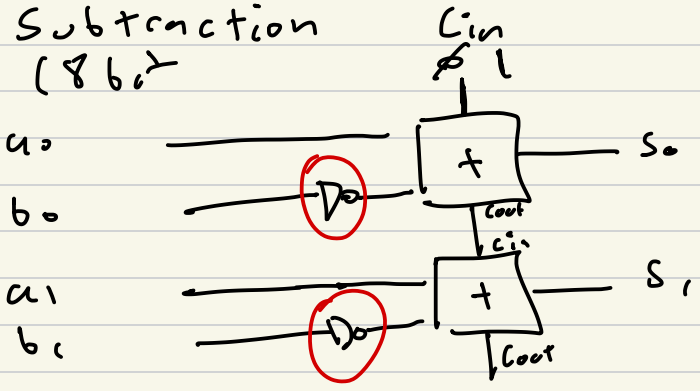


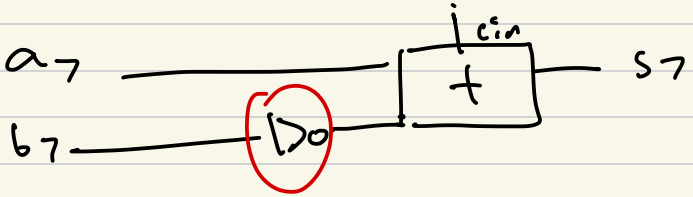
S_1	S_0	out
0	0	a
0	1	b
1	0	c
1	1	d

2 bit 2 input MUX



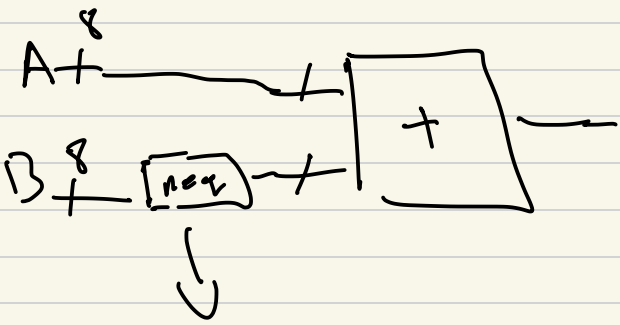
Subtraction (8 bit)

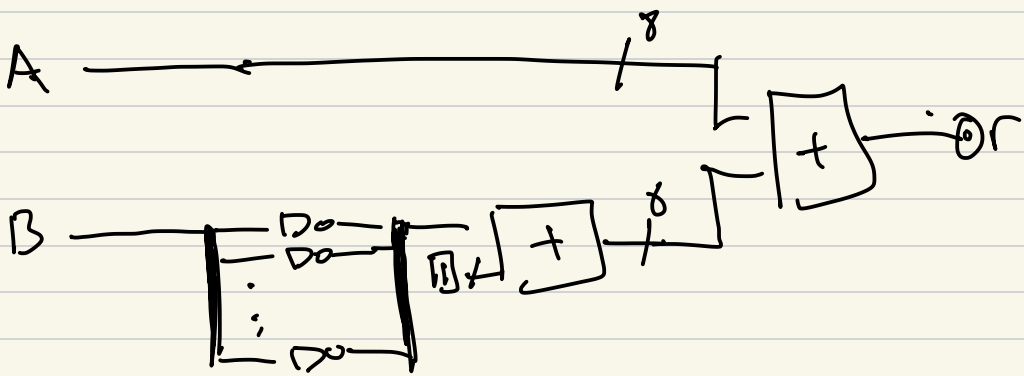




A - B

A + (-B)





Sequential logic